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EP 0786919 A1 EP 0721267 A2 EP 0708574 A2
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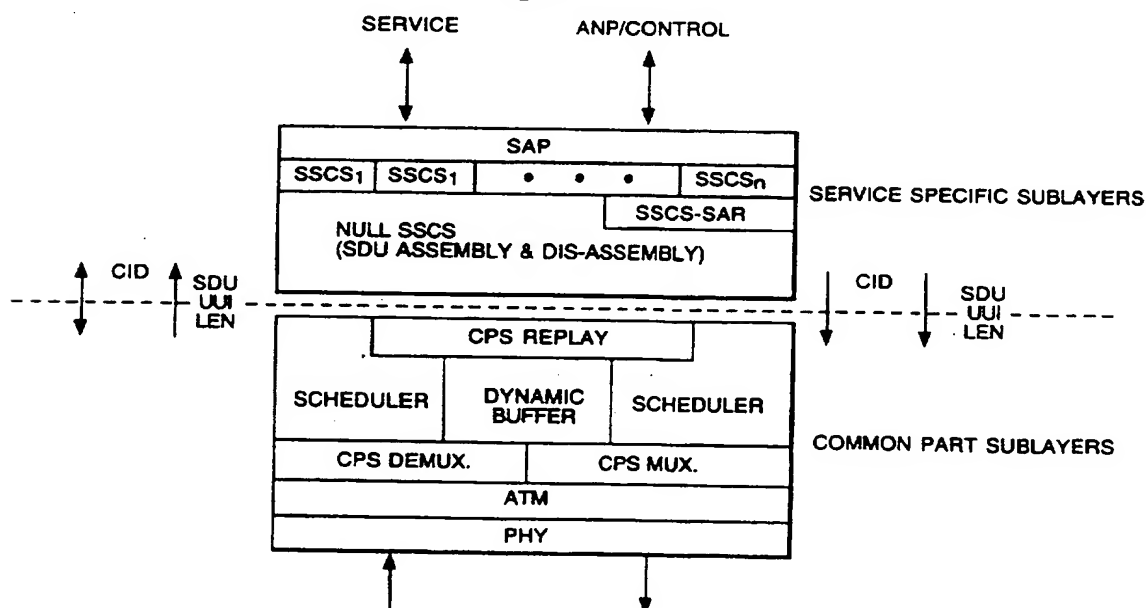
UK CL (Edition P) H4K KTK, H4P PPS
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(54) Abstract Title

Adaptation layer switching

(57) In an adaption layer switching network providing transport convergence (eg. the assembly of AAL-2 minicells into ATM cell format), functional partitioning provides a separation between service specific (eg. adaption of the user service to or from AAL-2 minicell) sublayers and common part (eg. adaption layer switching) sublayers. This enables the support of a range of SSCS functions via a common set of CPS blocks.

Fig.3.



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At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

The claims were filed later than the filing date within the period prescribed by Rule 25(1) of the Patents Rules 1995

Fig.1.

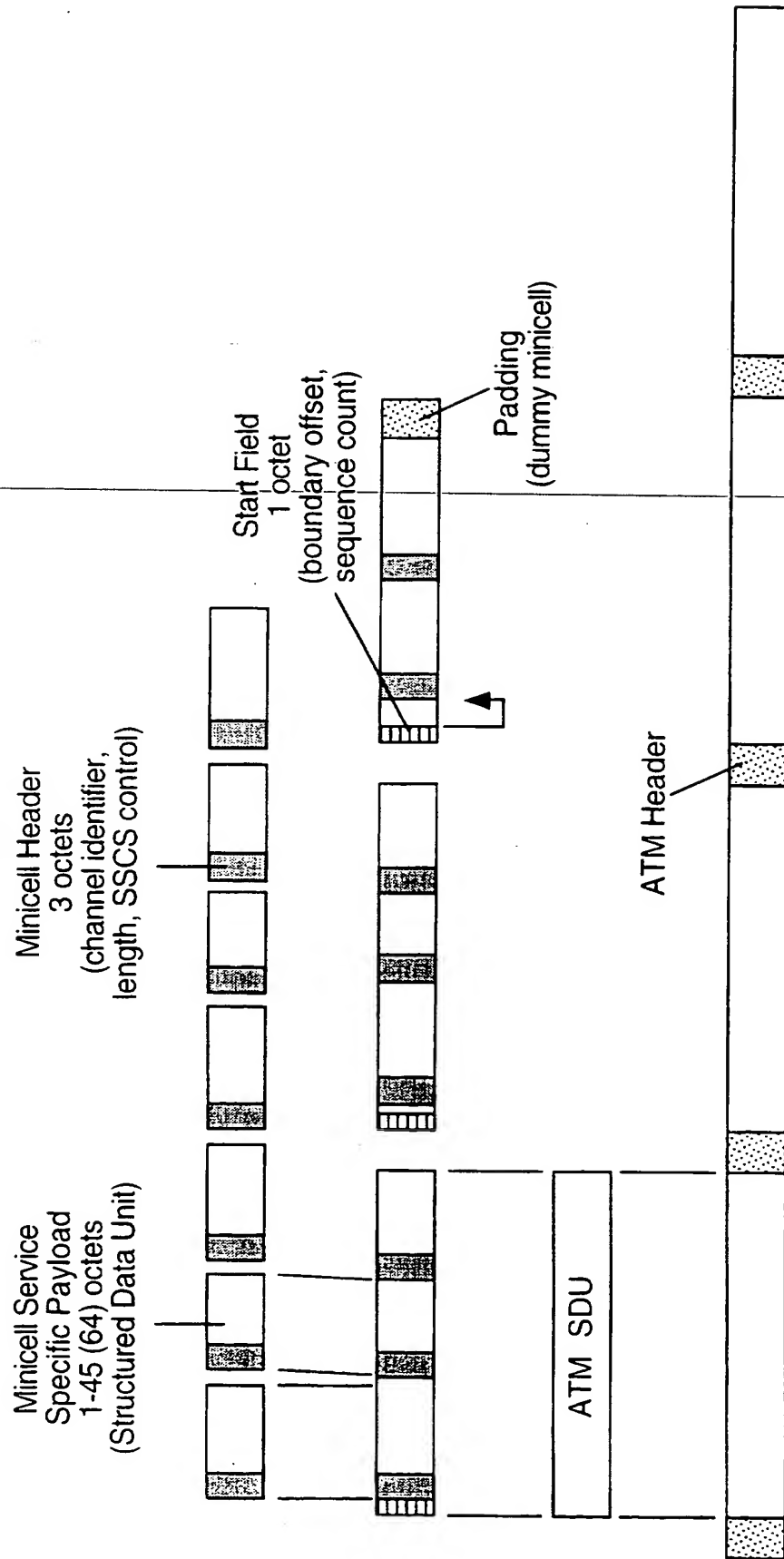


Fig.2.

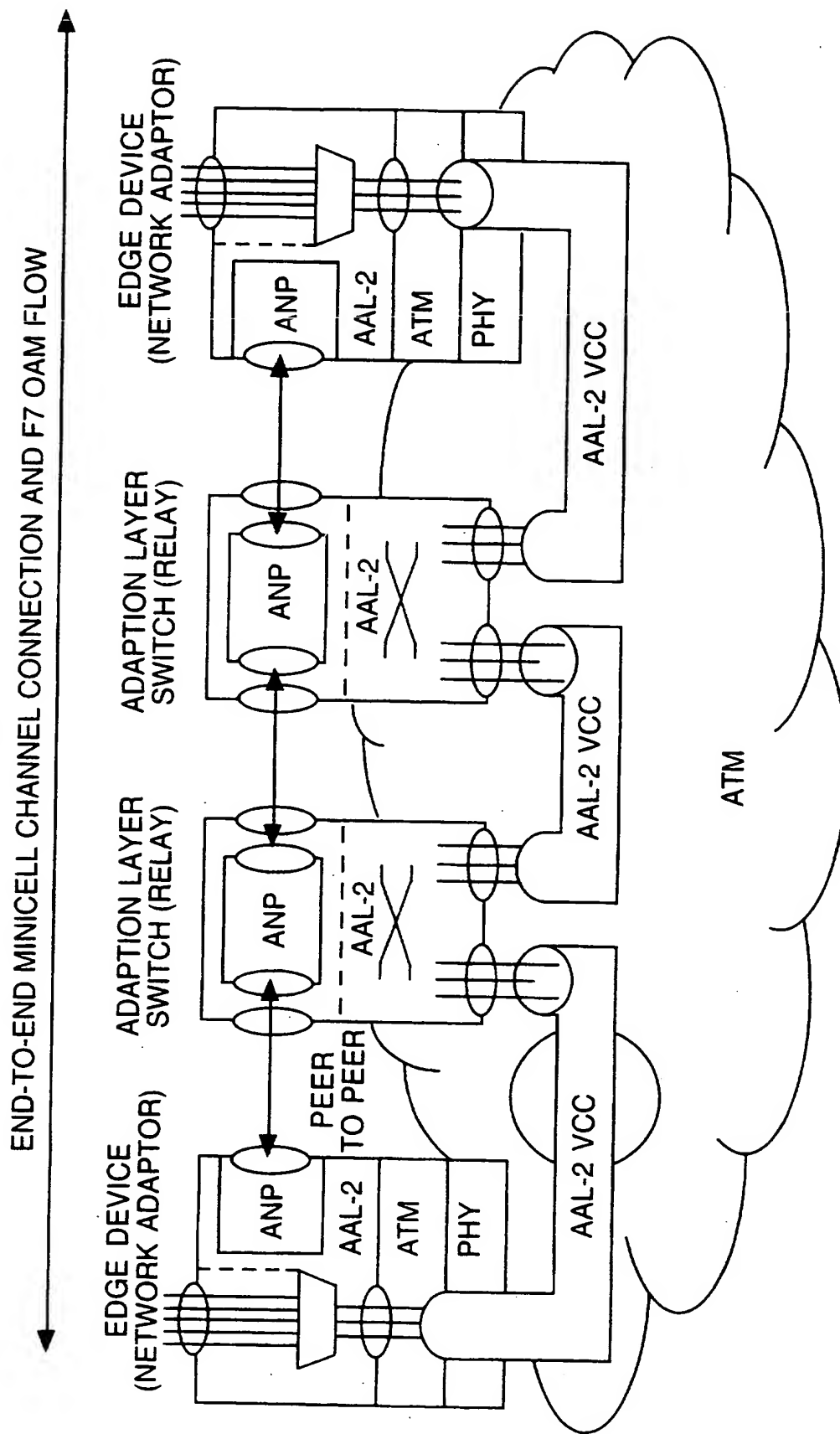
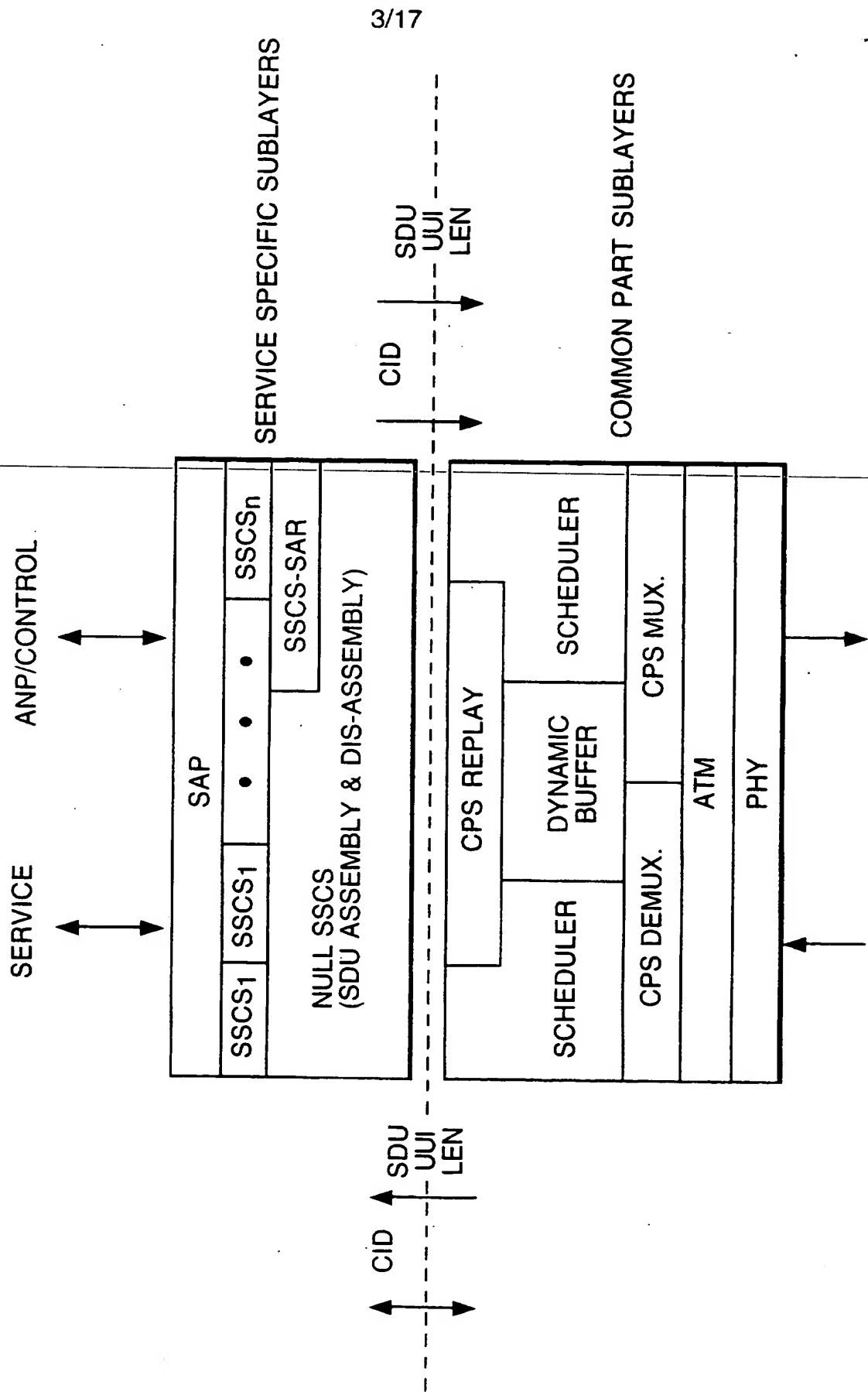
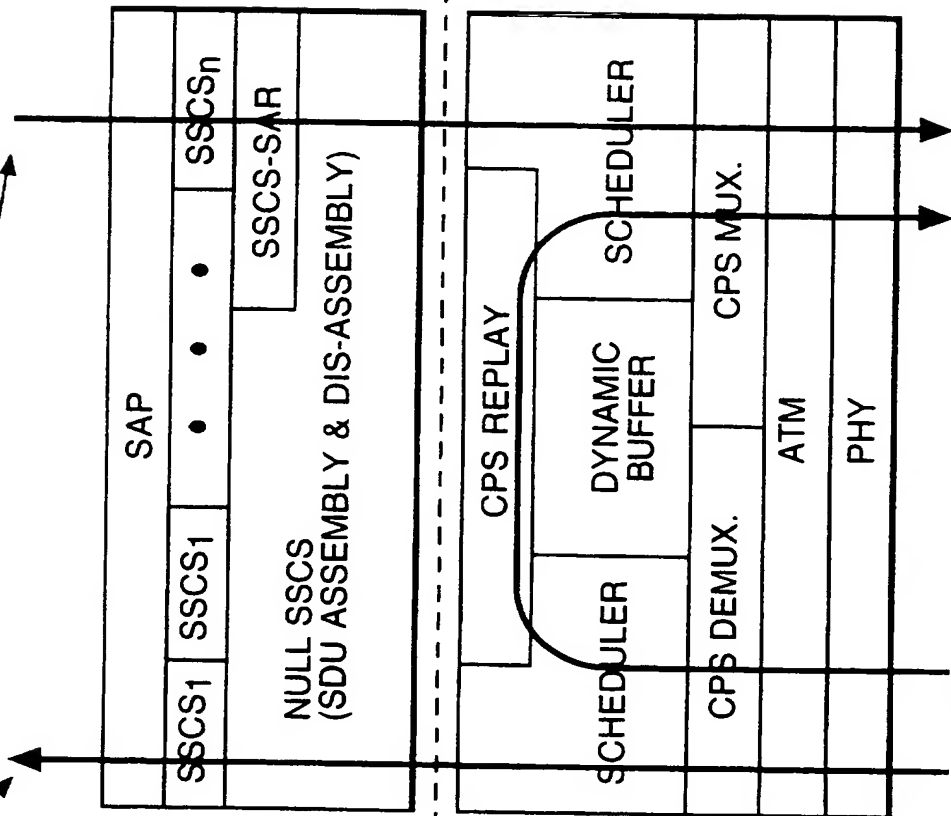


Fig.3.



SERVICE SPECIFIC
CONVERGENCE FUNCTION

Fig.4.



MINICELL RELAY
FUNCTION

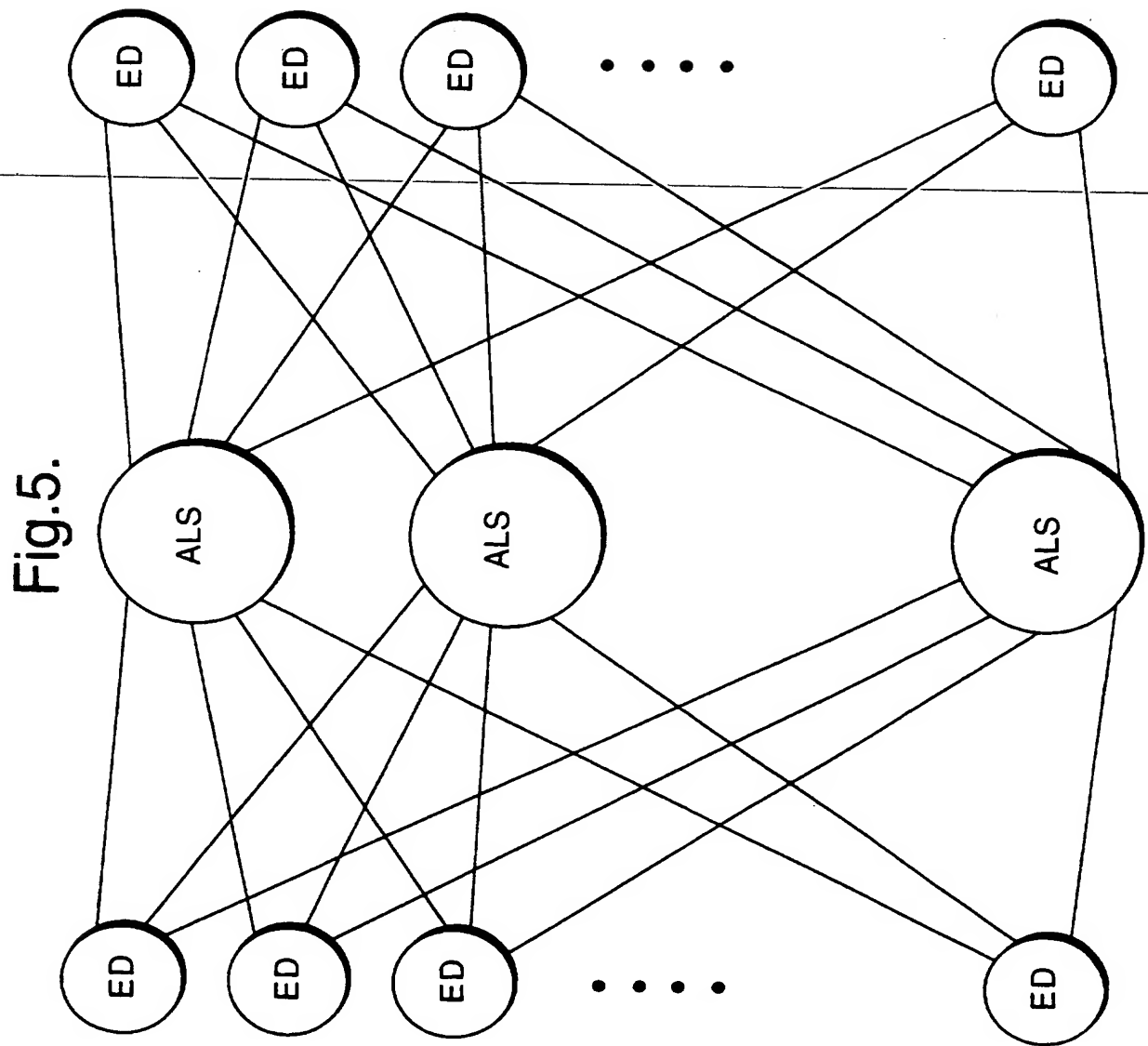


Fig.6.

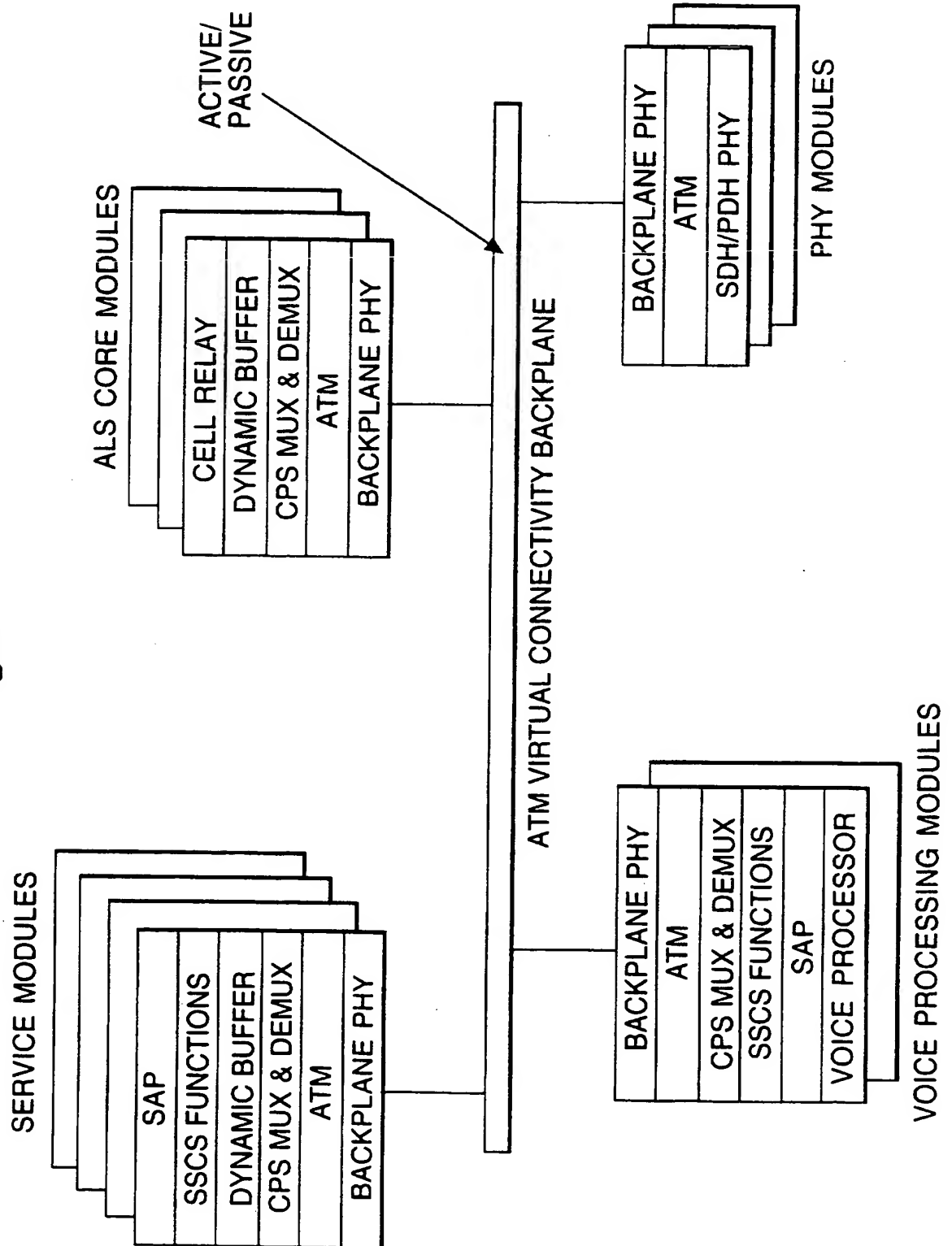


Fig.7.

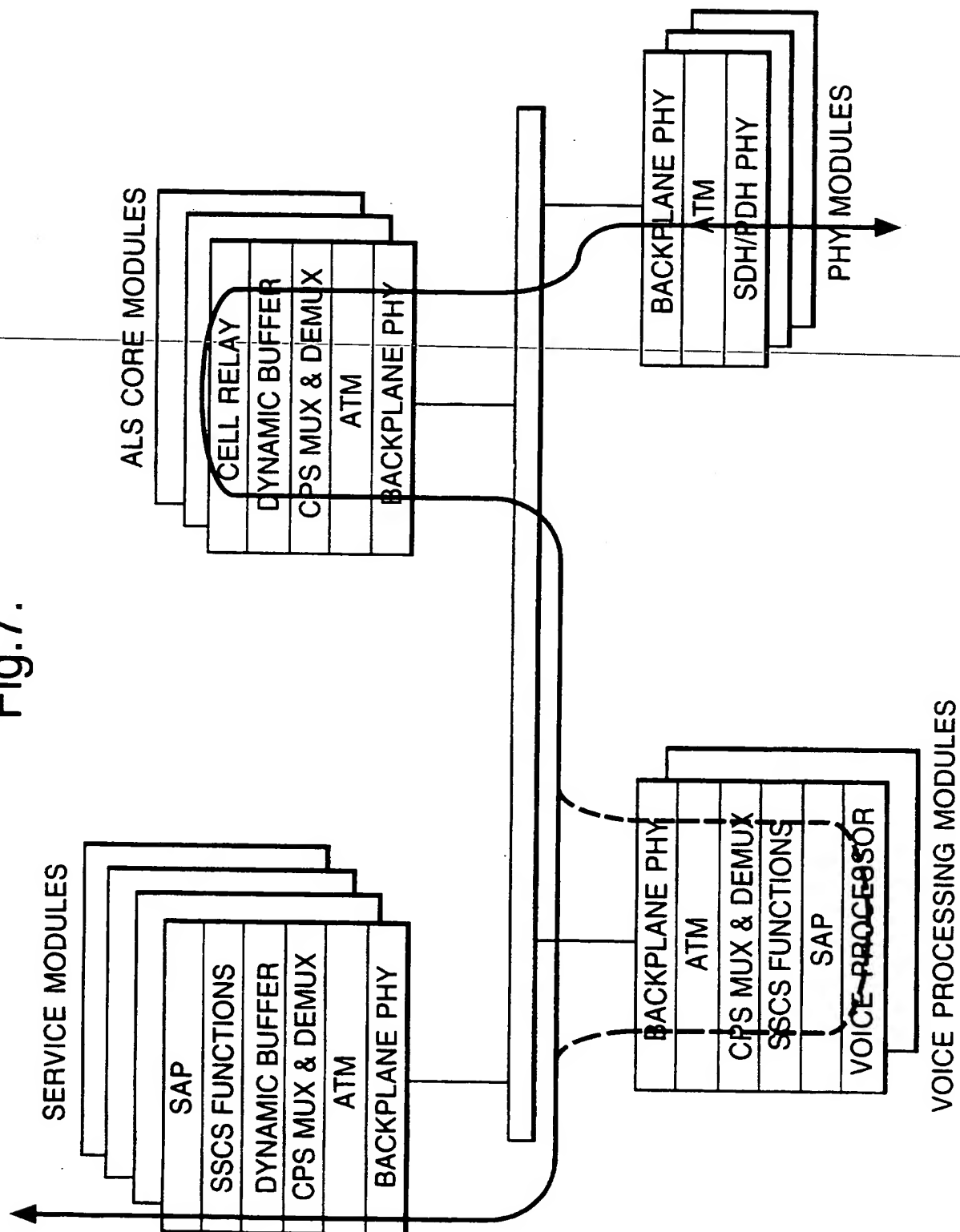


Fig.8.

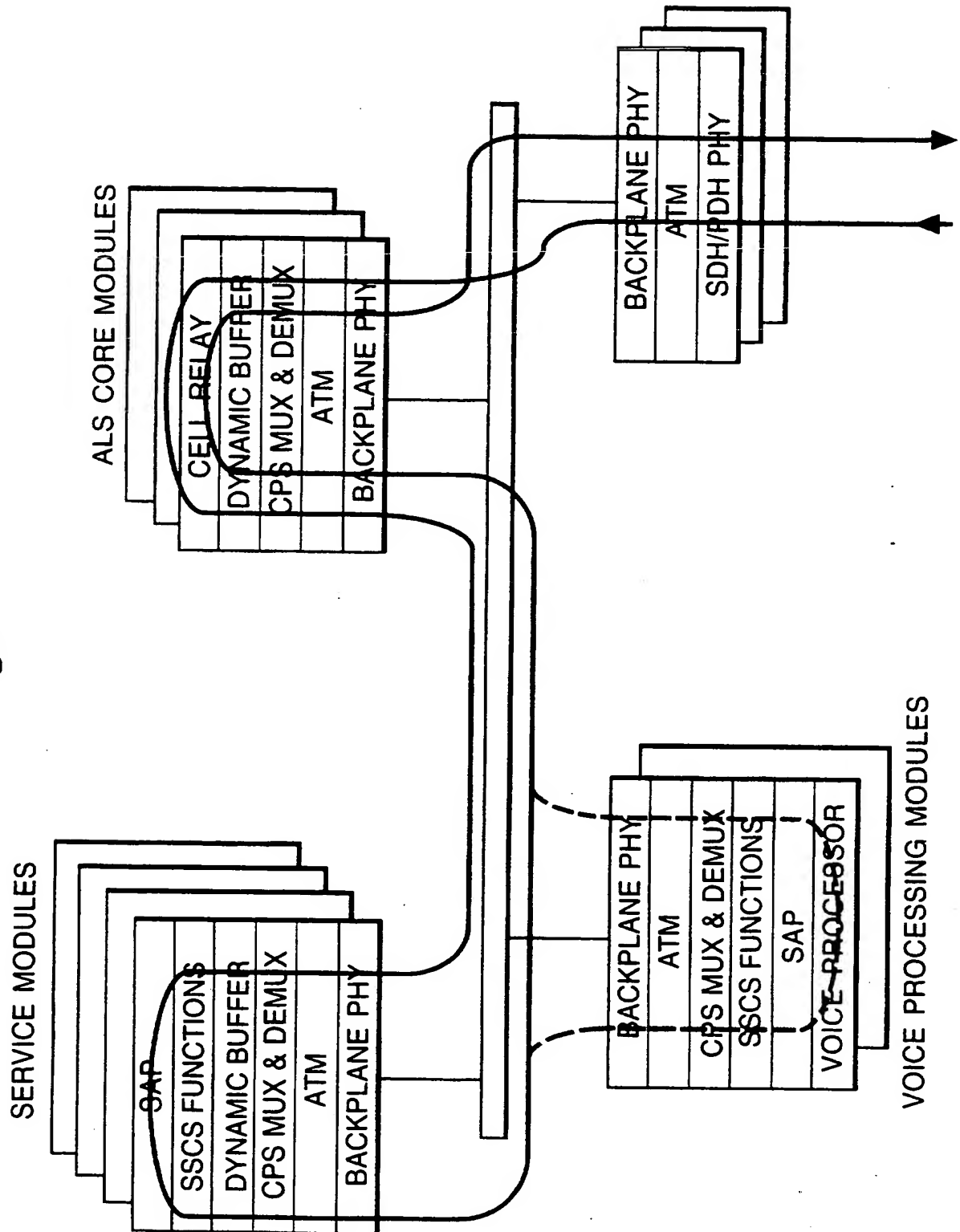


Fig.9.

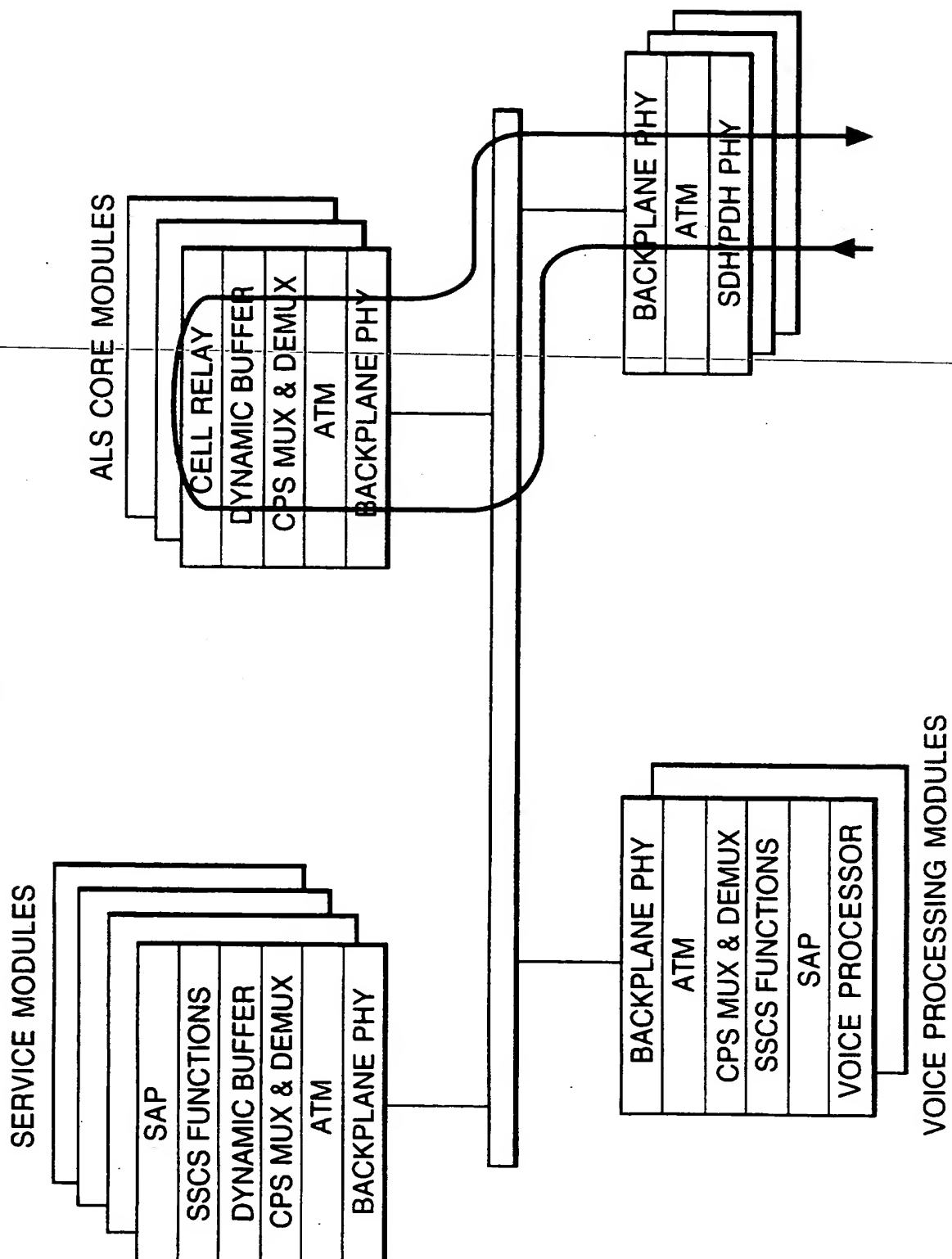


Fig.10.

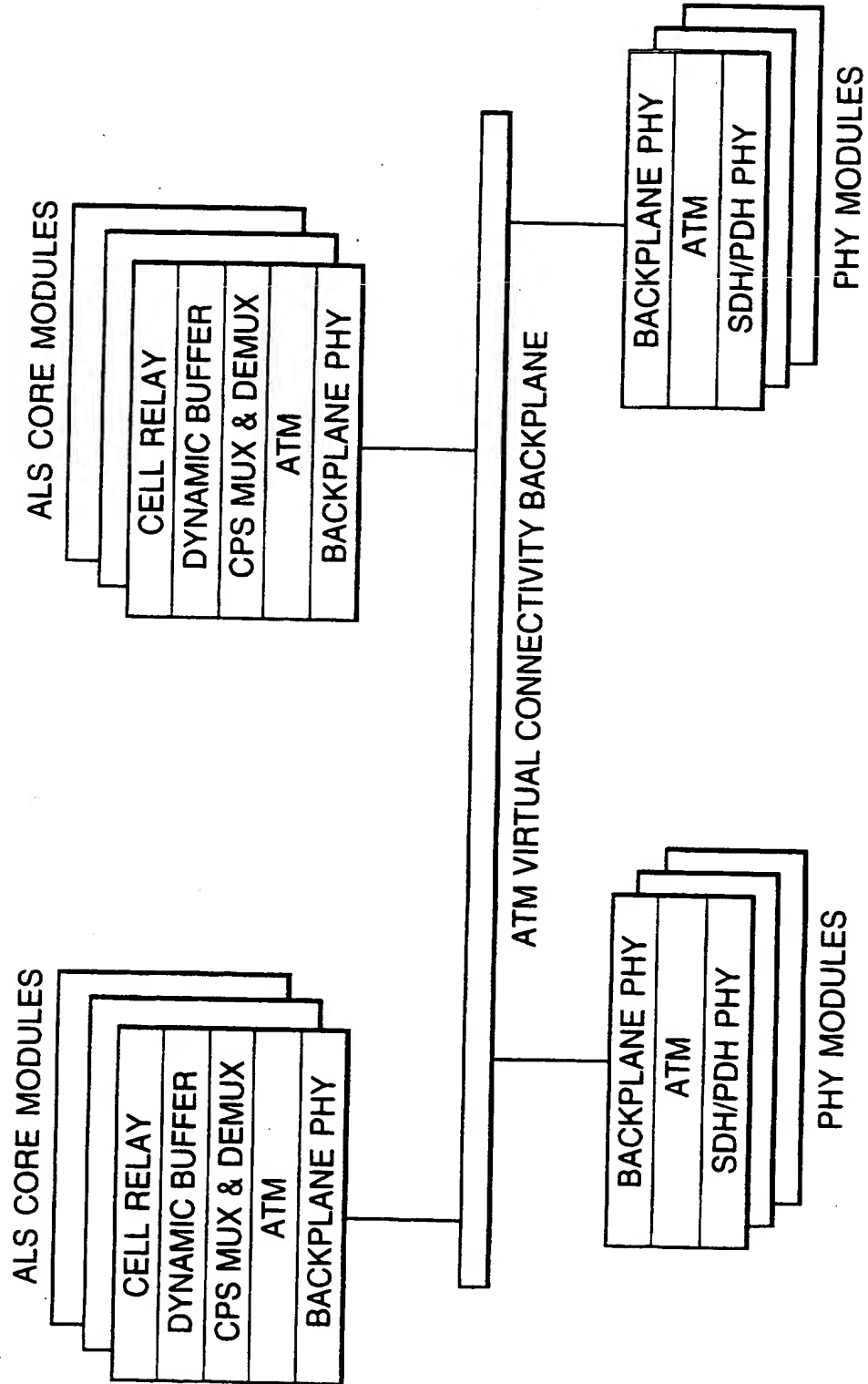


Fig.11.

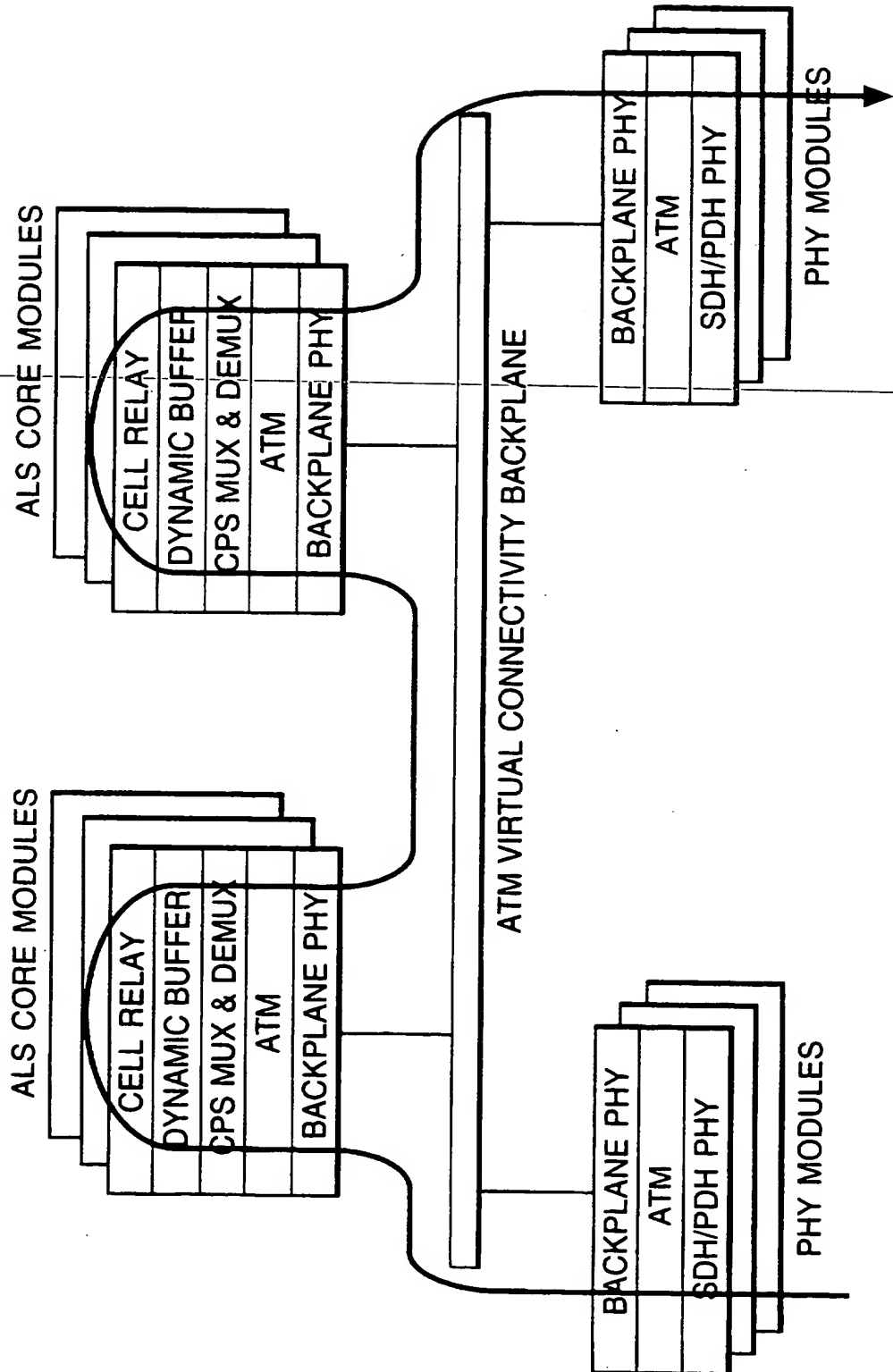
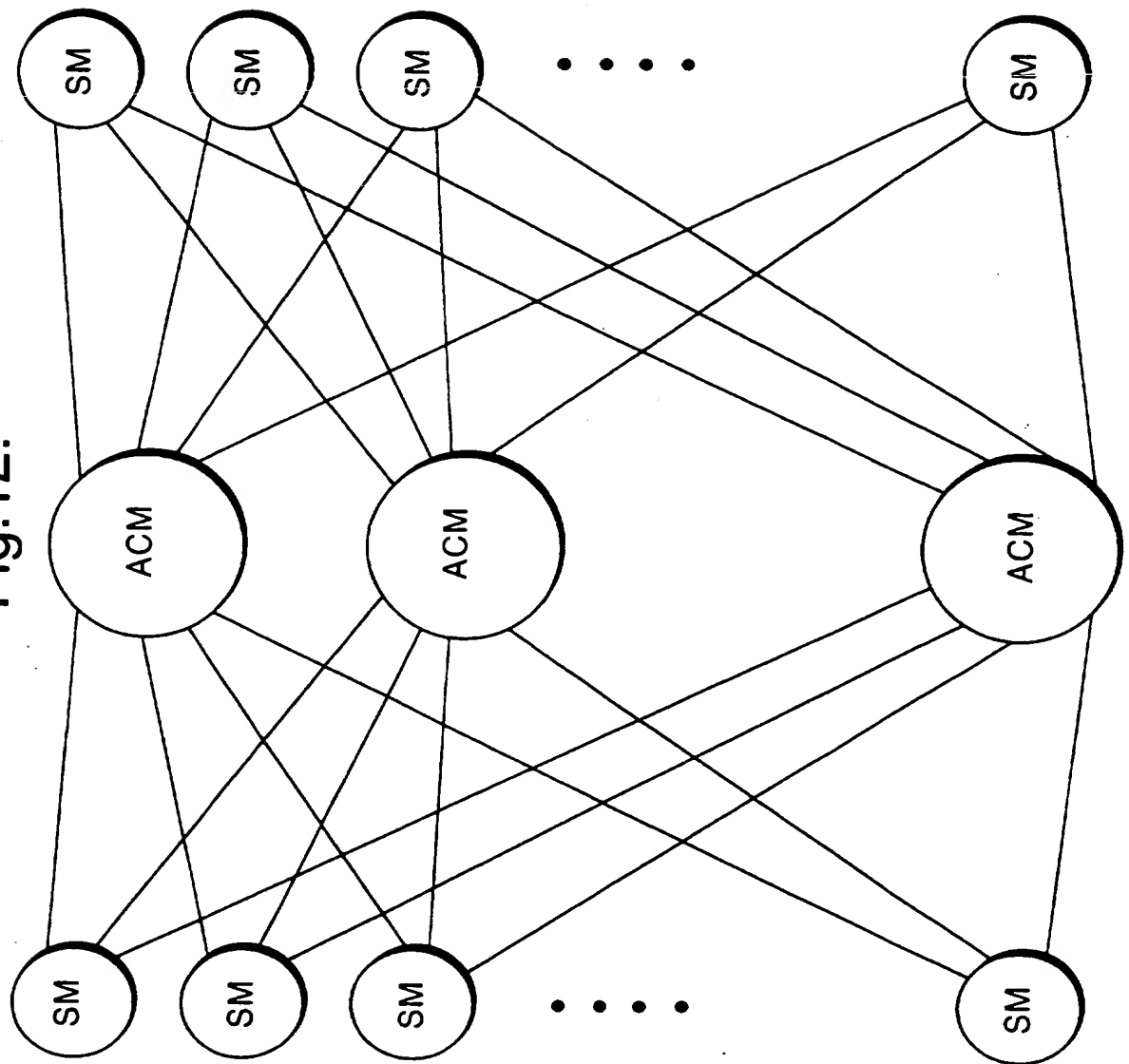


Fig.12.



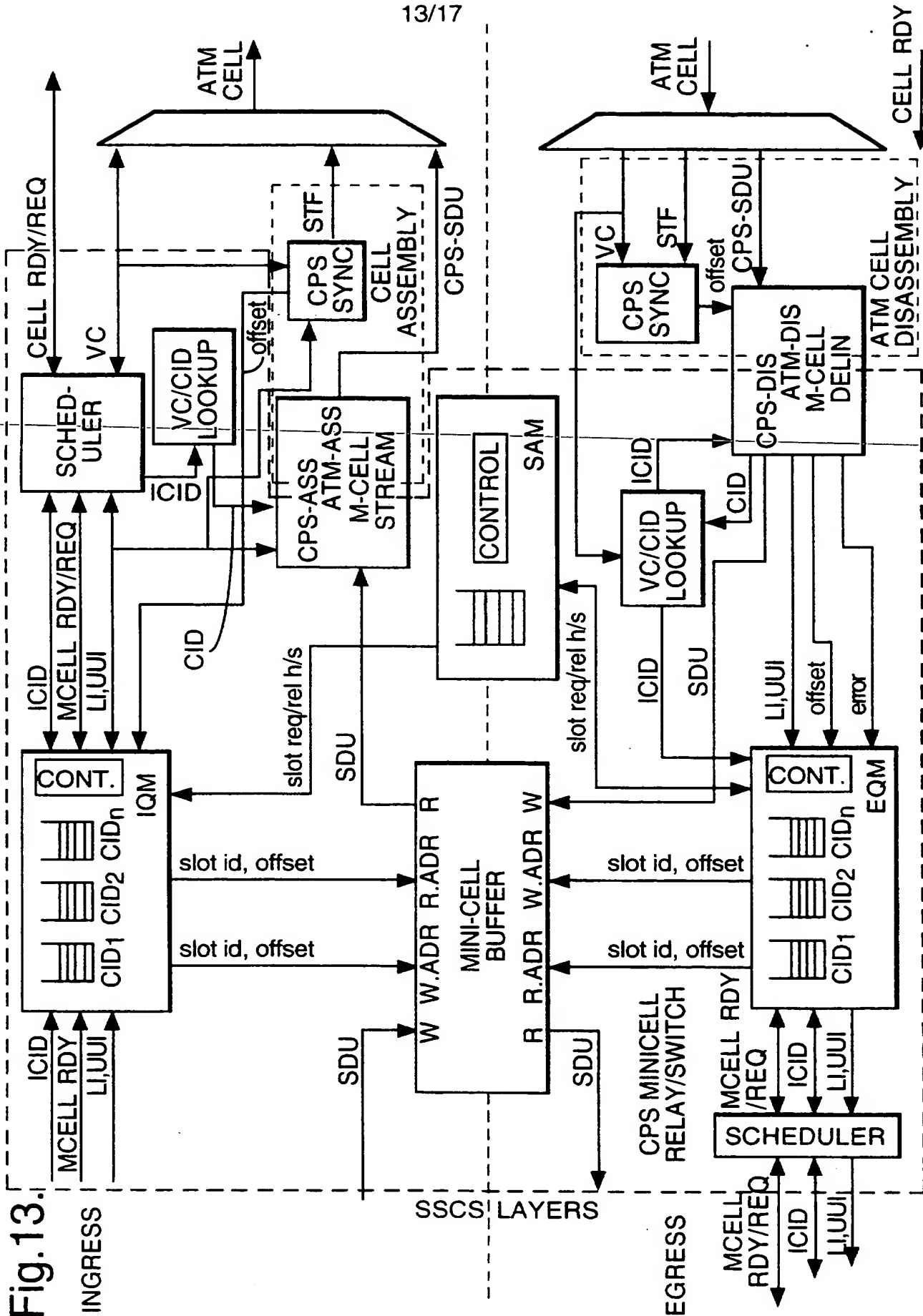


Fig. 14.

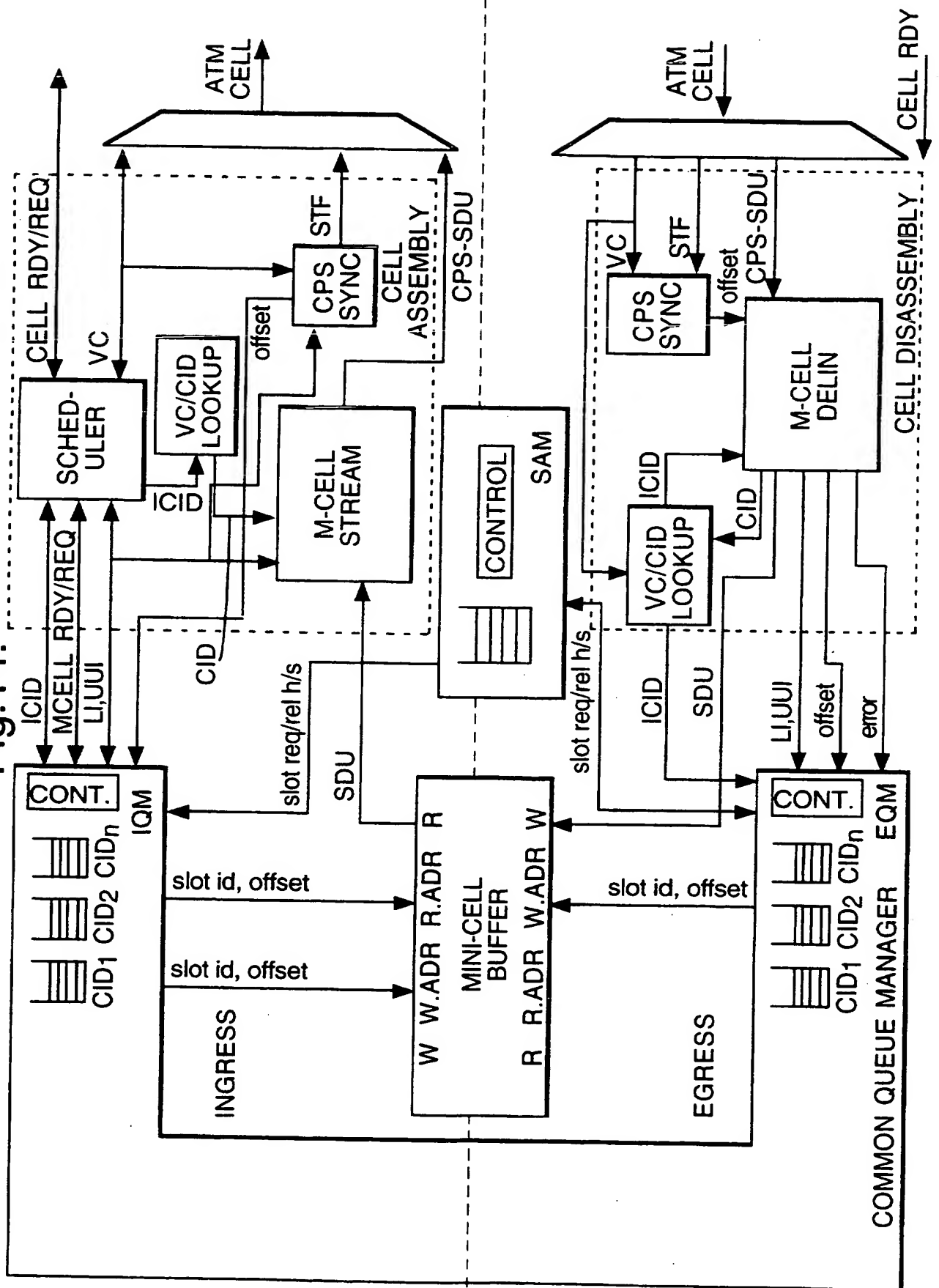


Fig.15.

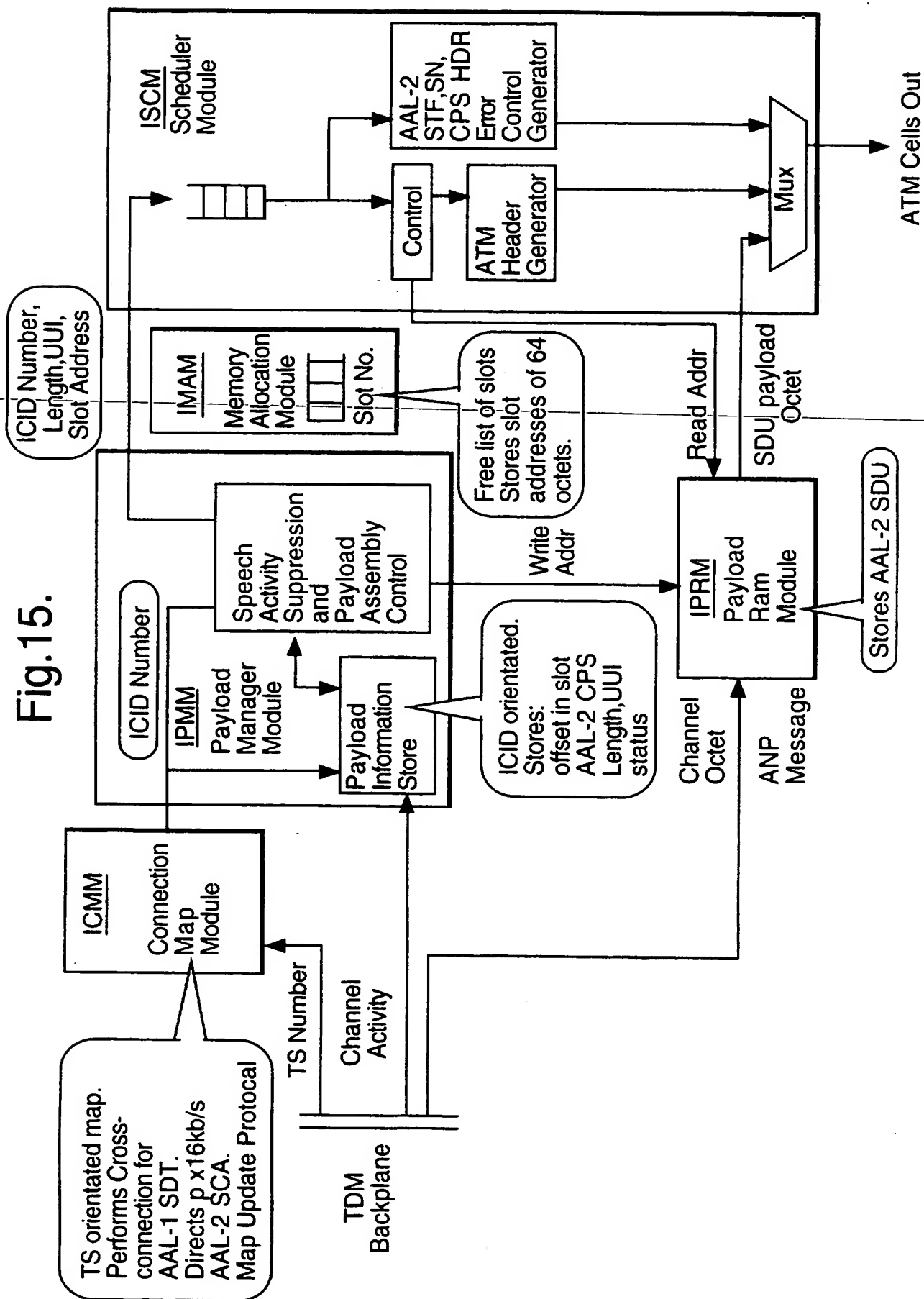


Fig.16.

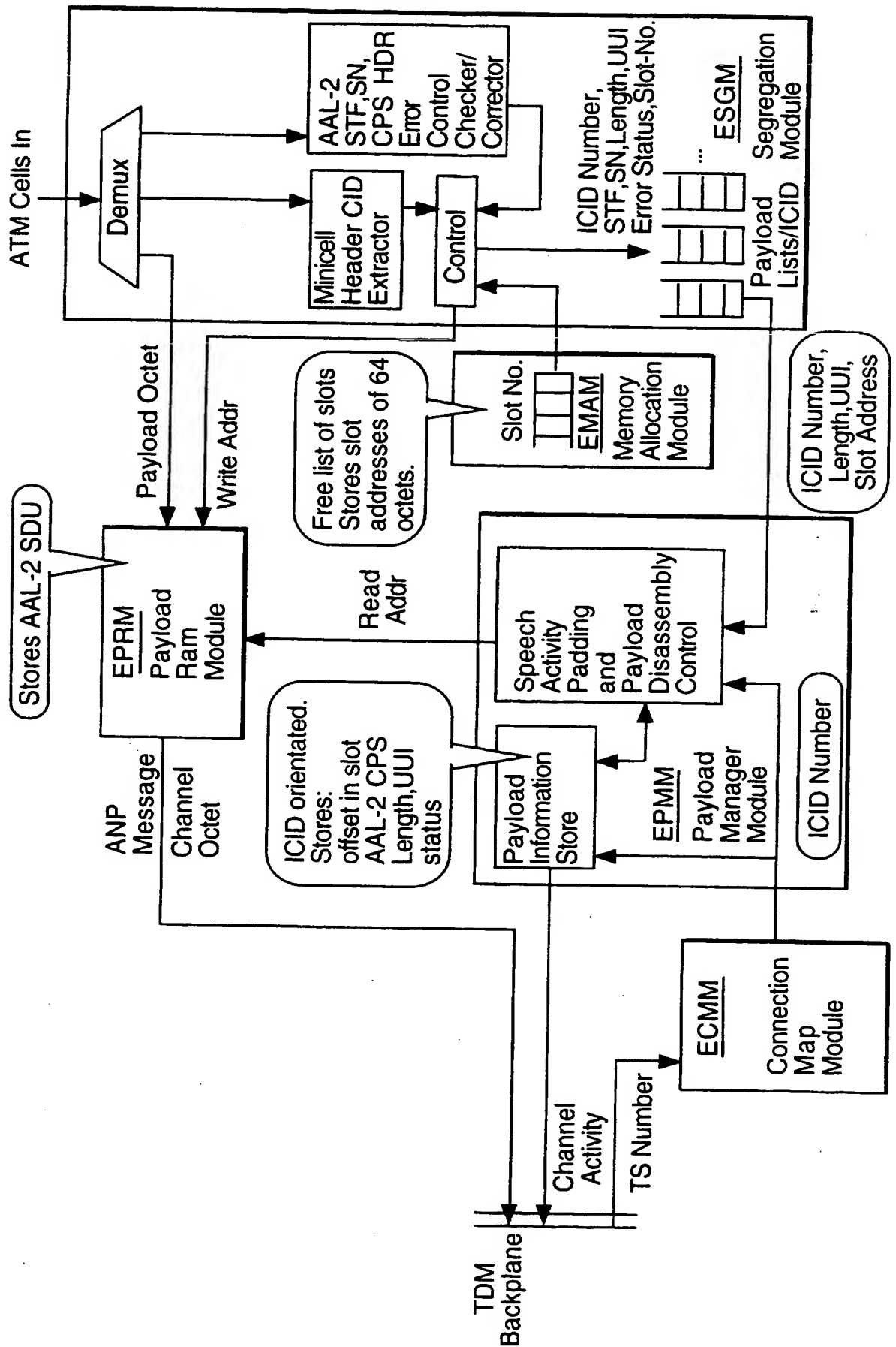
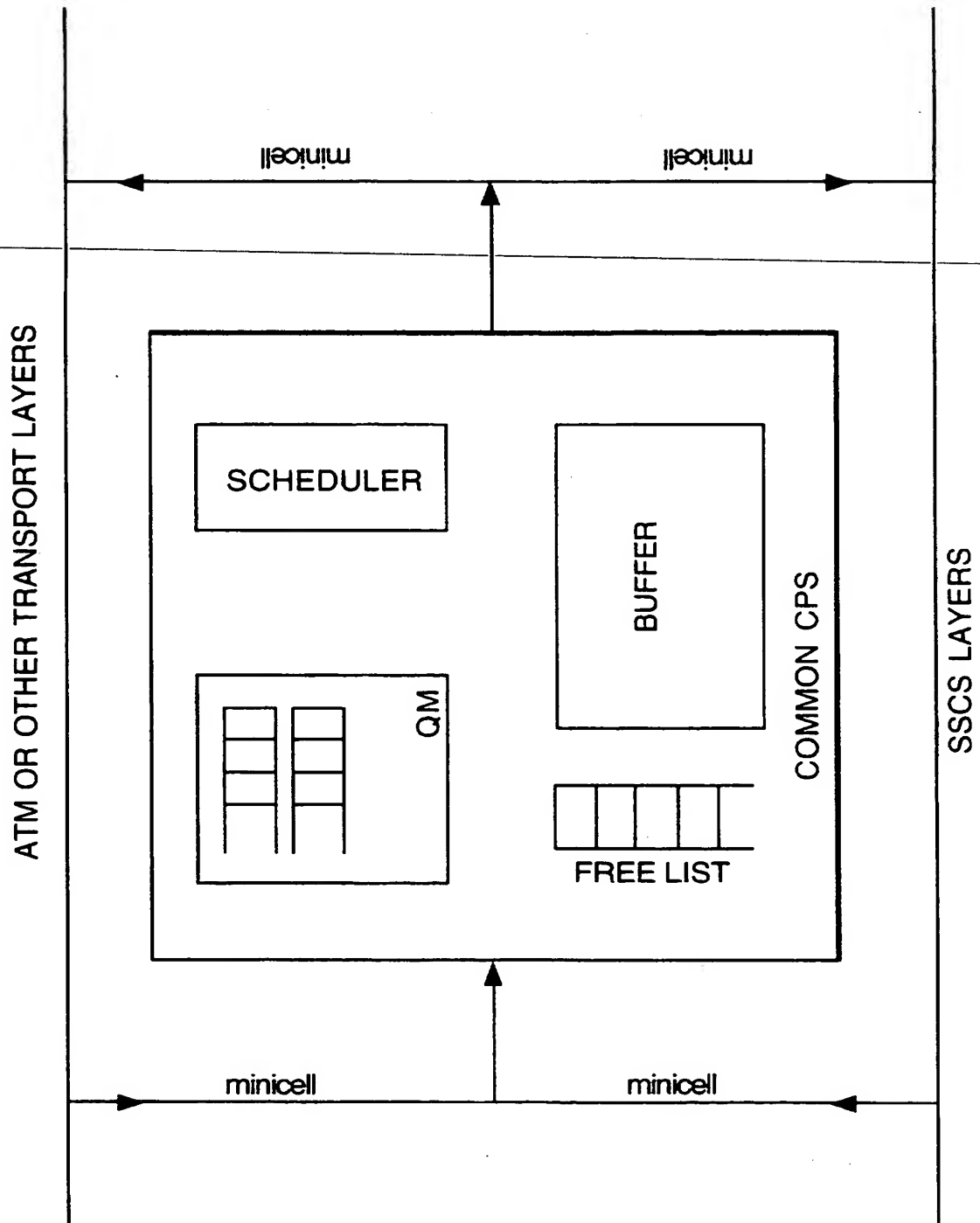


Fig.17.



ADAPTATION LAYER SWITCHING

This invention relates to digital communications systems and in particular to systems embodying asynchronous transfer mode (ATM) technology.

- 5 The asynchronous transfer mode (ATM) technology is a flexible form of transmission which allows any type of service traffic, voice, video or data, to be multiplexed together on to a common means of transmission. In order for this to be realised, the service traffic must first be adapted typically into 53 byte cells comprising 5 byte headers and
10 48 byte payloads such that the original traffic can be reconstituted at the far end of an ATM network. This form of adaptation is performed in the ATM adaptation layer (AAL).

- A recent development has been the introduction of the AAL-2
15 adaptation layer. This adaptation layer has been optimised to accommodate the demands of low bit-rate communications representing the increasing trend to greater voice compression. The adaptation layer is a multiplex of users in a single ATM connection where each user's information is carried in short packets or minicells
20 each with a header identifying the user channel and incorporating ancillary control information. This constitutes a dynamic trunk group of users in a single connection.

- As telecommunications networks increase in complexity and carry
25 increasing volumes of traffic, the current procedures for setting up connections between subscribers are limiting the performance of these networks. In particular, congestion may be caused by attempting to connect to a subscriber who is already busy, or by attempting to choose a route through an already congested part of the network. Thus
30 equipment and resources can be wasted in attempts to set up calls which cannot be completed. A further problem is that of scalability. As

the network expands to accommodate increased traffic and a larger number of subscribers, there is an increasing need to facilitate integration of new equipment into an existing network without simply increasing the congestion problem. Moreover, careful planning is required to ensure that calls can be routed through the network. This requires an ad-hoc distributed routing decision policy which limits the flexibility of the routing process as the call routing must be co-located with the switching node fabric.

Reference is here directed to our copending application (Reference S D Brueckheimer 19) of even date and which relates to the application of PNNI signalling to control an ATM adaptation layer switching network.

15 SUMMARY OF THE INVENTION

According to one aspect of the invention there is provided an adaptation layer switching network in which functional partitioning provides a separation between service specific sublayers (SSCS), common part sublayers (CPS) and transport convergence whereby to support a range of SSCS functions via a common set CPS blocks.

According to another aspect of the invention there is provided method of functional partitioning of an adaptation layer switching network by providing a separation between service specific sublayers (SSCS), common part sublayers (CPS) and transport convergence whereby to support a range of SSCS functions via a common set CPS blocks.

According to a further aspect of the invention there is provided a telecommunications network comprising edge device nodes and adaptation layer switching nodes, wherein the edge nodes terminate the adaptation layer switching nodes to service access points, and wherein the adaptation layer switching nodes provide minicell switching points within the network.

The network architecture for adaptation layer switching is derived from AAL-2 technology. An adaptation layer switching network provides the capability to deliver a fully scalable network and nodal solutions that can utilise existing ATM infrastructure for transport. The use of AAL-2 technology and adaptation layer switching will provide a network infrastructure suitable for

carrying all delay sensitive and real-time services with a GoS that meets ITU standards for delay and distortion. The network can be constructed from two basic building blocks - edge devices and adaptation layer switches.

The arrangement and method exploit the ATM adaptation layer (AAL-2) to
5 configure networks and switching functions. In particular, the AAL-2 adaptation switching function is employed to provide the ability to establish and control an AAL-2 minicell connection across many nodes thus forming an adaptation layer switching network. The network can readily be scaled to
10 global proportions.

The arrangement and method also provide a functional partitioning of AAL-2 to realise the necessary functions for a switching network. These functions include a service specific convergence function (SSCF) and a minicell switching/relay function. Thje partitioning achieves a clear separation
15 between the SSCS, CPS and transmission convergence (TC) sublayers, and enables a common CPS to support a multiplicity of SSCS functions and a full range of transmission media.

BRIEF DESCRIPTION OF THE DRAWINGS

An embodiment of the invention will now be described with reference to the
20 accompanying drawings in which:

25 Figure 1 illustrates the multiplexing of minicells into ATM;

Figure 2 is a schematic diagram of an ATM network
illustrating end to end minicell connection and traffic flow;

30 Figure 3 illustrates AAL-2 functional partitioning to provide a service specific convergence function;

35 Figure 4 illustrates data paths through thre functional partition of figure 3;

Figure 5 illustrates the ALS network architecture;

Figure 6 illustrates the modular partitioning of an edge device;

5 Figure 7 is a schematic diagram showing a core data path through an edge device of figure 6;

Figure 8 is a schematic diagram showing an ancillary data path through an edge device of figure 6;

10 Figure 9 is a schematic diagram showing an alternative ancillary data path through an edge device;

Figure 10 shows the modular partitioning of an ALS node of the network of figure 5;

15 Figure 11 shows an ALS node data path;

Figure 12 is a schematic diagram of a stand-alone single node;

20 Figure 13 illustrates a VLSI architecture for

Figure 14 illustrates a VLSI architecture for

Figure 15 illustrates AA-2 ingress anatomy; and

25 Figure 16 illustrates AA-2 egress anatomy; and

Figure 17 shows a common integrated CPS.

30 DESCRIPTION OF PREFERRED EMBODIMENT

The AAL-2 adaptation layer has been optimised to cope with the demands of low bit-rate communications, representing the increasing trend to greater voice compression. The adaptation layer is a multiplex of users in a single ATM connection, where each user's information is carried in a short packet or minicells, with a header identifying the user channel with ancillary control information. This is illustrated in figure 1.

By sharing the fixed length payload of the ATM cell between users, the compromise of trading cell assembly delay for bandwidth efficiency is neatly side-stepped, a sacrifice which would be acute at low bit-rates and on expensive leased lines. AAL-2 adaptation equipment performs a concentration function to ensure high utilisation, but can also limit the holdover delay of traffic when usage is low.

A further feature of minicells is that they may be of variable size, from 1 to 64 octets, to accommodate a wide variety of applications with minimal overhead. Thus the mapping to ATM cells is asynchronous and in fact quite independent of the length of an ATM cell. The boundary of minicells in the ATM cell payload is signified in every cell by a start field (STF), which specifies the offset, and thus minicells form a self-delineating flow.

The minicell is structured so that services of different types can be supported as Service Specific Convergence Sublayers (SSCS), all carried over the minicell Common Part Sublayer (CPS) identically. The minicell header includes channel identity, length and User-to-User Information (UUI), the latter allows the functions of an SSCS to be specialised according to purpose.

For example four successive samples of ADPCM at 32 kb/s could be packetised into a single mini-cell to provide a packetisation delay of just 1 ms. The octets could form a minicell payload directly, and in this case the SSCS has null functionality. Alternatively a data frame, such as GSM mobile packets, are typically much greater than 64 octets, so a Segmentation and Reassembly (SAR) SSCS function supports such application. The SAR function can be assisted by using the UUI field between adaptation entities to ensure proper sequenced reassembly of the data packet.

Minicells provide a universal adaptation medium able to support voice, video and data in a common ATM VCC.

The set-up, maintenance and clear-down of minicell channels in an AAL-2 connection, and the switching operation of the relay, is controlled by the AAL-2 Negotiation Procedures (ANP). AAL-2 connections are supported by in-band F7 OAM minicells, replicating for the adaptation layer the connection maintenance capabilities of ATM.

The AAL-2 standard specifies a feature that allows minicells to be relayed between connections, without the need to terminate the carried service (see figure 2). The original objective of this capability was to solve a problem in wireless networking, whereby a mobile-to-mobile call is preferably established without transcoding to PCM, to avoid the detriment to quality and cost. The initial connection is established across a single relay or switching centre. However with the mobility of the terminal, the connection may proceed through a succession of handovers thereby requiring an end-to-end minicell channel connection through several nodes.

Having once established a minicell switching layer, then it is available to be used for many other applications. This capability is exploited to provide the ability to establish and control a minicell channel (adaptation layer) connection across many nodes thus forming an Adaptation-Layer-Switching network.

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AAL-2 Functional Partitioning

This section describes a functional partitioning of AAL-2 technology that enables the service specific convergence function (SSCF) - adaptation of the user service to and from AAL-2 minicells - and a minicell switching functionality to be realised in an efficient and manner. Further this partitioning enables the SSCF and ALS switching functions to share much common technology.

Figure 4 shows the AAL-2 functional partitioning which provides the two key functions required for an adaptation layer switching network: the SSCF and the minicell switching function. The data paths through the functional partition are shown in figure 5. It shows the SSCF and ALS functions. By using the functional partitioning, the subject of this invention, enables the two functions to share much common technology.

30

A description of the functional layers is listed below , explaining the key functions of each layer:

PHY LAYER

Σ the physical interface between the ATM AAL-2 cells and the underlying physical medium, considered to be any suitable physical telecommunications bearer fit for the purpose.

ATM LAYER

Σ assembly and disassembly of ATM AAL-2 cell payloads (ATM-SDUs) into ATM cells

5 Σ includes the functions of ATM header generation and error protection and detection and translation/substitution of VP/VC addresses

Σ those skilled in the art will recognise that ATM can drive an ATM Forum UTOPIA bus or equivalent

10

AAL-2 CPS MUX/DEMUX

Σ assembly and disassembly of AAL-2 minicells into an ATM SDU

15 Σ generation/extraction of the STF field (sequence number, parity and offset) and any other such standardised functions

Σ segmentation/reassembly of minicells (minicells can be carried over successive ATM cells)

Σ VC/CID translation function

Σ minicell multiplexing and demultiplexing function

20 Σ generation/extraction of minicell header CPS information (including minicell header error detection and protection)

DYNAMIC BUFFER/CELL RELAY

Σ maintains per VC/CID queue of minicells

25 Σ minicells SDUs stored in a slotted shared memory or output queued paradigm

Σ per VC/CID queue manager maintained for ingress and egress functions

Σ minicell scheduling

30 Σ either ingress or egress scheduler can operate in master or slave mode

Σ in slave mode ingress scheduler (throughout this paper ingress denotes the side that generates ATM cells) is slaved to an *ATM data request* function issued by the ATM LAYER - in master mode the ingress scheduler generates *ATM data ready* instructions to the ATM layer

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- Σ ingress scheduler maintains a per AAL-2 VC holdover delay timer to ensure a maximum CPS multiplex delay and QoS is met - can invoke an automatic payload padding function
- Σ in slave mode egress scheduler (egress denotes the side that receives ATM cells) is slaved to an SSCS scheduler - in master mode the egress scheduler generates minicell ready commands to the SSCS layers
- Σ per VC/CID queuing structure enables the ingress and egress schedulers to offer multi-priority AAL-2 connection ability to enable different QoS capabilities
- Σ minicell relay function
 - Σ switches minicells from the egress to ingress functions in order to accomplish the adaptation layer switching function by making egress queues available to ingress so as to form a common memory switch in the adaptation layer.

SSCS Functions

- Σ assembly and disassembly of minicell data packets in a service specific manner (the service could be TDM, asynchronous packet or synchronous packet based).
- Σ generation/extraction of SSCS control information (e.g. UUI bits, length and OAM)
- Σ multiplexes/demultiplexes user minicell packets with control (ANP) and management minicell packets in synchronous or asynchronous form
- Σ an SSCS function can support synchronous (e.g. PCM), semi-synchronous (e.g. ADPCM with speech activity) and asynchronous services (e.g. GSM mobile packet)
- Σ several SSCS instances can operate in parallel each tailored to a particular service
- Σ some common SSCS functions (e.g. segmentation and reassembly - SAR - of long data packets) may be common to several SSCS functions
- Σ functionality of SSCS is dependent on the service supported but may include functions such as SAR, SAD, error coding and recovery (e.g. use of minicell sequence number and payload error protection), jitter compensation, plesiochronous frame slip/stuff operation, channel concentration, coding rate adaptation (e.g. 64kb/s to 32 kb/s due to

congestion), CDV compensation or any service specific error mitigation functions, or service related function

5 **SAP - Service Access Point**

Σ describes the interface between the SSCS layers and the particular service delivery mechanism

ALS Network Architecture

- 10 In this section we describe the network architectures that can be configured arising from the functional partitioning discussed above. The adaptation layer switching network architecture is shown in figure 3. Figure 3 highlights the adaptation layer nodes. The connectivity is provided by Switched and Permanent VCs (SVC/PVC) in the ATM layer, which has not been shown,
15 but behaves as a virtual connectivity backplane.

The network is built using two types of nodes an Edge Device (ED) node and an Adaptation Layer Switching (ALS) node. The ALS nodes perform a switching function in the adaptation layer and thus route AAL-2 minicells across the network. The minicell switching is performed in the adaptation
20 layer - there is no service termination performed in the ALS. Service termination is performed in the ED nodes - the ED provide a service specific convergence function (SSCF) - adapting the service to and from AAL-2. Using differing SSCF instances ED can simultaneously support many differing service types - the QoS provided to each user can be tailored to
25 their service requirements. Thus the adaptation layer switching network forms a full service capable network - it can support all real time and non-real time services offering a QoS equivalent to today's ITU networks.

ED and ALS nodes share much common technology and can both be configured from cascadable, collocated, and commonly controlled and
30 managed physical devices. Large nodes (and hence networks) can be built using cascadable VLSI building blocks and hence an ALS network can scale from a small size to global proportions in a cost effective manner. Using 0.5 um VLSI technology ALS nodes that can support the order of a million 64kb/s circuits and an order of 10s of millions of low-bit-rate voice
35 connections can be built!

Many differing network configurations can be derived using the core ALS technology. Small networks can be configured by inter-connecting EDs to each other directly. The addition of the ALS switching nodes enables the network size to be dramatically scaled. It is possible to configure networks that utilise several stages of ALS (nodal) switching - however the inherent nodal and network scalability of ALS technology also means that it is possible to scale the network to global proportions (hundreds of millions of connections) by using just a single stage of ALS switching as illustrated in figure 3. The simplicity and symmetry of the single-stage switching network shown allows straightforward congestion management using both load-balancing and rejection of blocked traffic at source as per co-pending PNNI case. This yields the highest bandwidth utilisation, from a minimum sufficiency of ALS nodes, to meet any QoS targets on call blocking. The ALS nodes can be designed to be fully non-blocking nodes to improve throughput, and ensure stable behaviour under overload conditions. A fully interconnected ED-to-ALS mesh has been shown in figure 3 however it is equally possible to configure networks that use a subset of this connectivity.

Module Partitioning

In this section we describe how ED and ALS nodes can be configured in a modular fashion using simple cascadable building blocks derived from the AAL-2 partitioning described above. The modular building blocks described below all share much common technology.

Figure 6 shows the a generic modular partitioning of an ED node. It consists of a set of cascadable building blocks - service modules, voice processing modules, ALS core modules and PHY modules. The modules are interconnected using ATM transport - the ATM provides a virtual connectivity backplane which may be an active switch or passive connectivity.

30

The key building block in an ED node is the service module (SM) which performs the SSCF (adaptation of service information to and from AAL-2). In its simplest form an ED node could be configured using a single SM. Using 0.5 um VLSI technology an SM that supports several thousand low-bit rate user channels can be integrated into a single component device. To increase the size of an ED node SMs are cascaded together. To scale the node (and hence network) further ALS Core Modules (ACM) are added. An ACM performs the minicell switching function and using current (e.g. 0.5

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micron) VLSI technology an ACM that supports tens of thousands on low bit rate channels can be integrated into a single component device. Again ACMs can be cascaded together in parallel to increase the switching capacity. Using ACMs in an ED node removes the requirement to fully interconnect all SMs to all routes in the network by functioning as AAL-2 tandem switching points.

Also shown in figure 6 are PHY modules that interface the node to the network transport medium (for example SDH or PDH), and optional voice processing modules (VPMs). The VPMs can be used to perform additional voice processing functions for example compression, echo cancellation and silence detection where the interface to the VPMs is via AAL-2 minicells using the appropriate SSCS function of VLSI.

Figure 7 shows the core data path within an ED. User information is (de)adapted into minicells in a service specific manner. The minicells can be optionally routed to a VPM for additional voice processing before being routed to the ACM. The ACM routes the minicell into the network (via a PHY module).

The modular partitioning shown however provides the ED node with much flexibility and a number of additional data paths can be supported. Figure 8 shows how the ED can be used to perform a 'grooming' function whereby incoming minicells are routed into an SM where an SSCF conversion is performed (mapping one SSCS to a differing SSCS) before re-routing the resultant minicell back to the network. Again optional additional voice processing functionality can be performed via the VPM.

Figure 9 shows how the ACMs in an ED can be used to perform a network minicell switching function. In this manner a single physical ED node can perform the logical functionality of both the ED and ALS nodes. This is very useful particularly when configuring smaller network solutions.

To scale the network further (up to global proportions) a single stand-alone stage of ALS nodes can be added to the network. The generic modular partitioning of the ALS node is shown in figure 10. The node is shown 'unfolded' to illustrate the logical use of a double bank of ACMs (and associated PHY modules). This double switching bank enables very high

switching fan out to be achieved - an incoming minicell on one of the VC supported on any one of the ACMs can be switched to any of the other ACMs (in the next bank) where it can be switched onto any one of the network facing VC's that it supports. This is illustrated in figure 11.

5

Single Fabric Switch

The combination of SM and ACMs described above can also be configured to form a stand-alone single node solutions. The nodal configuration is shown in figure 12. It consists of a fully interconnected mesh of SM and ACMs. The fully interconnected mesh guarantees that load balancing can be applied across all VC's and thus the node provides strict sense non blocking performance. The configuration described above could be used as a plug-replacement for the connectivity provided by a current generation narrowband (synchronous) switch (and offers equivalent QoS for 64 kb/s). Further such a switch can also support a full mixture of subrate and full rate services in an efficient manner, and can also support additional semi-synchronous and synchronous services. The inherent scalability of the modular technology enables a node that can support several hundred thousand narrowband connections to be supported.

VLSI Architecture

In this section a generic VLSI solution that delivers the SSCF and minicell switching functions is described.

The VLSI architecture comprises the following principles:-

- 25 Σ a Service Access Point (SAP) that is the association between the adaptation layer and synchronous/semi-synchronous/asynchronous delivery of user information,
- Σ a Dynamic Circuit/Packet Switch that performs: a concentration function by dynamically mapping circuits or packets to/from AAL-2 VCs and minicell channels; a cross-connection function for exchange between optional voice processing devices; and a multi-casting capability (this is an SSCS function);

30

- Σ an AAL-2 Segmentation and Reassembly (SAR) function that exchanges circuit/ packet based user channels to and from the payload of minicells(this is an SSCS function);
- Σ a dynamic buffer management function that forms a common shared memory architecture to provide: a dynamic amount of buffering per AAL-2 VC and minicell channel; plesiochronous buffer control; cell delay variation compensation; and the adaptation layer space switching matrix (the dynamic buffer is part of the CPS);
- Σ an AAL-2 multiplexing, demultiplexing and switching control function that operates on the dynamic FIFO queues in the buffer (this is an CPS function);
- Σ and an ATM multiplexing, demultiplexing function that interfaces to the network or an ATM backplane and forms the ATM Service Access Point (SAP).

15

Figure 13 shows a block diagram of the generic partitioning of the VLSI architecture. Only the core part sub-layer technology is shown in this diagram. The SSCS functionality is service dependent (an example SSCS partitioning for synchronous and semi-synchronous services is described in the following section).

20

The structure of figure 13 is split into three parts - the ingress side (generates ATM cells) the egress side (receives ATM cells) and a common dynamic buffer and control. The dynamic buffer is used to store the minicells. It is organised as indirected linked lists of equally sized slots of memory. The difference between the head and the tail of the list is effectively the amount of stored information per minicell channel ID per VCC. This can converted into units of time for synchronous services according to the service type, the packet size and bit-rate represented. A dynamic buffer is required for AAL-2 because, although for a DBR service the Cell Delay Variation (CDV) has a fixed maximum, the number of users per AAL-2 VCC is able to vary dynamically, so the buffer size is required to vary as a function of the number of configured users. For synchronous services a constant mean time difference is maintained between head and tail. For plesiochronous compensation, this is monitored for slowly changing trends and a slip or a stuff function by an amount appropriate to the service is invoked to meet

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standards requirements. For CDV compensation this is achieved by setting the time difference slightly in excess of the amount of configured CDV, and is monitored frequently. A training algorithm determines the smallest cell transfer delay (minimum CDV or earliest cell) which is unchanging under load. Thus only lost or late minicells need be compensated by detecting the onset of buffer underflow, and using the previously described stuff mechanism (compensation is an SSCS function).

The minislot dynamic buffer is controlled by the Slot Allocation Module (SAM). This maintains a list of the free slots available in the buffer. New slots are assigned to the ingress and egress and old slots reclaimed through the use of a simple handshake procedure between the SAM and the ingress and egress queue managers respectively.

The operation of the egress and ingress processes are now described in more detail starting with the egress functionality.

ATM cells transporting AAL-2 minicells are received at egress. The ATM demultiplexing function strips the ATM header from the payload. The header HEC information is processed to ensure the header is valid - it is not the whole of the cell is junked. The header VCI/VPI information is processed and the VC identifier passed to the cell payload disassembly process (the architecture is capable of supporting many VC's in parallel). The ATM payload is also forwarded to the cell payload disassembly process.

The first function performed by the payload disassembly process is the CPS synchronisation function (CPS SYNC on the diagram). A key feature of AAL-2 is that minicells are transported asynchronously over the ATM payload so in general the start of a cell will contain the remainder of a minicell transported in the previous ATM cell (of that VC stream). The CPS SYNC function must ensure that the reassembly of the two minicell parts occurs successfully. Since the length of the minicell is always known (through the LI field of the header) the number of octets expected in the remainder is also known. However, ATM cell loss or error could cause misconnection of minicell parts to occur so the AAL-2 process includes a start-field (STF) with every ATM cell to prevent this. The one octet STF contains an offset (effectively denoting the length of the minicell remainder in the ATM payload) and a single-bit sequence number to enable detection of lost ATM cells (the STF is error

protected via a single bit parity). Thus the function of the CPS SYNC is to process the STF field and in normal operation it will verify that the minicell remainder is the expected remainder (i.e. it verifies that its expectation of the offset is the same as that sent in the STF). If an error is detected then an error status signal is generated, the part minicell stored in the dynamic buffer may be discarded and minicell disassembly begins at the next minicell boundary contained in the ATM cell payload. The error status allows an SSCS layer to mitigate the error in a service profile manner.

The disassembly of the minicells from the ATM cell payload is performed by the minicell delineation function (MCELL-DELIN). This processes the ATM payload, extracting the minicell packet header information and minicell payloads (SDUs). The MCELL-DELIN performs error detection on the minicell headers - the remainder of the payload may be discarded on detection of an error. The detected minicell CID together with the VC is used to determine a unique identifier for the VC/CID combination (ICID). The ICID is used to store the minicell payload in the appropriate queue in the dynamic buffer (the buffer may maintain a queue for each VC/CID stream or use fewer queues depending on the service relationship between minichannels). The extracted minicell SDUs are written into the minicell buffer under control of the egress queue manager (EQM).

The EQM maintains the minicell queue for each VC/CID stream. New minicells are written to the tail of the queue - old minicells are read into the SSCS functions (or CPS if relay) from the head of the queue. (The minicell SDUs are stored in the dynamic buffer thus the EQM must maintain a list of slot identifications (or buffer addresses) where the SDUs are located for each VC/ID stream. Additional control information is also stored in this list by the EQM including the length of the minicell SDU (LI), the user-to-user bits (UUI), and any error status. These fields are extracted from the minicell packet headers by the MCELL-DELIN function and passed directly to the EQM.

When a complete minicell packet has been written into the dynamic buffer the EQM signals this to the egress scheduler via the ICID and MCELL RDY (minicell ready) flags. The egress scheduler can operate in either master or slave modes. In master mode the egress scheduler schedules the dispatch of minicells into the SSCS functions. This is useful for asynchronous or

semisynchronous services which may perform their own buffering. The order of dispatch can of course differ to the order that minicells are received according to QoS criteria. To dispatch a minicell the scheduler sends a ICID and MCELL-RDY flags to the SSCS functions and simultaneously sends the ICID and a MCELL-REQ (request) to the EQM. The EQM will then control the reading of the minicell SDU from the dynamic buffer (the LI and UII information is also passed across to the SSCS functions). The minicell is taken from the head of the relevant queue and once read the slot is relinquished back to the SAM. In slave mode, e.g. for synchronous or semi-synchronous services, the egress scheduler acts transparently - forwarding MCELL RDY and MCELL REQ flags between the EQM and the SSCS layers. (In slave mode the receipt of a minicell is indicated to the SSCS layer and the SSCS layers determine when to request this minicell - this enables the dynamic buffer to be used by the SSCS layers for compensation of CDV, jitter and plesiochronous behaviour when supporting synchronous or semi-synchronous services.

The ingress process shares much commonality with the egress process. It accepts minicell packets from the SSCS layers and assembles them into ATM cells for transport across the ATM network.

Again the dynamic buffer is used to store the minicells prior to dispatch. The SSCS signals the availability of minicell data to the ingress process via the ICID and MCELL RDY flags. The minicell SDU is written into the dynamic buffer under the control of the ingress queue manager (IQM). The IQM operates in a manner entirely analogous to the EQM.

The availability of a minicell is signalled to the ingress scheduler by the IQM. The egress scheduler resides in the ATM cell assembly block. Again the scheduler can operate in both slave and master mode. In slave mode the assembly of minicells is slaved to the ATM layer. Thus the ATM layer will request an ATM PDU for a particular VC and the scheduler will begin its assembly immediately. This mode is particularly useful if the VC connections are true CBR connections - thus ATM cells for a particular VC are dispatched at regular intervals irrespective of the minicell loading of that VC. In master mode the scheduler dictates the dispatch of ATM cells according to a pre-defined scheduling algorithm (according to QoS criteria). The scheduling algorithm will be designed to provide a desired per VC QoS. In general the

scheduler will maintain timers per VC to ensure that the AAL-2 holdover delay parameter is met. Whether in slave or master mode the scheduler has the capability to instigate a padding function to allow the dispatch of partly filled ATM cells.

- 5 Under control of the ingress scheduler minicell SDUs are read from the dynamic buffer. Since the IQM maintains a per VC per CID linked list of available minicells with this architecture it is a simple manner to have many differing levels of minicell priority multiplexed into a single VC. The ATM payload is assembled in the cell assembly block which again shares much
- 10 commonality with the cell disassembly block. In particular both a VC/CID lookup function is performed (to translate the ICID to the minicell CID) and a CPS-SYNC function that synchronises the segmentation of a minicell over successive ATM payloads. The assembly of the minicell packets and ATM payload is performed in the MCELL-STREAM function that performs the
- 15 inverse of the MCELL-DELIN function found in the egress. The MCELL-STREAM generates the minicell packet headers from the CID, LI and UII information (including EDC information), and multiplexes this with the SDU data to form the minicell stream which together with the STF field formed by the CPS-SYNC function forms the payload of the ATM cell.
- 20 The ATM payload together with the VC information is used to generate a complete ATM cell by the ATM cell multiplexing function.

In figure 13 the ingress and egress functions have been separated and shown independently. Further the a partitioning between the ATM cell assembly/disassembly and the CPS minicell relay/switch function is shown..

- 25 Those skilled in the art will recognise that the ATM cell assembly/disassembly blocks could be replaced with blocks defined to support any other transport structure (for example MPEG-TS frames) - the minicell switch/relay block remains identical. Further the ingress and egress parts of the minicell switch/relay function can also be made into a single
- 30 silicon macro sharing common blocks serving both flow directions.

Minicell Switching

The description above described the action of the CPS layers when implementing the SSCF function. However the technology is equally applicable to performing the minicell relay or switching function. When performing the minicell switching function the minicells received at egress immediately form the minicells being queued at ingress - effectively the IQM and EQM functions are collapsed into a single function by tying the ingress egress and ingress scheduler together. This is illustrated conceptually in figure 14. The minicell switch does not therefore need to maintain a separate ingress and egress queue when performing the minicell switching function.

- 5
- 10 The previous section described a general embodiment of the CPS partitioning suitable for supporting all service types. In this section we describe by way of example a specific embodiment of a VLSI chip to perform the service convergence function for synchronous and semi-synchronous sub-rate services. In particular (although not restricted to) the invention is designed to support ADPCM (at rates down-to 16 kb/s) with or without speech-activity-detection (SAD) according to ITU G.726. The ingress and egress functionality of the VLSI ASIC is shown in figures 15 and 16.
- 15

The ingress function is first described. Incoming service data is written into the ASIC in a synchronous manner and assembled into minicell packets under control of a connection map module (ICMM) mapping timeslots to ICID. The synchronous user data is written into the payload of the relevant minicell packet. This process is controlled by the payload manager module (IPMM) which controls the minicell payload assembly process and performs additional functions including SAD. SAD is driven by the channel activity signal which signifies the silence/speech status. Minicells SDU are assembled in the payload RAM module (IPRM). This is a dynamic memory and a control module (IMAM) controls the allocation and de-allocation of slots, large enough for the largest minicell, in this memory.

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- 30 Completed minicells are assembled into ATM cells under action of the scheduler module (ISCM). This block performs scheduling, CPS assembly, STF assembly, minicells multiplexing and the ATM cell header generation functions.

On egress ATM cells are demultiplexed in the egress scheduler module (ESGM). This controls the disassembly of minicells. Minicell SDUs are

written into the payload RAM module (EPRM). The scheduler maintains a per CID linked list queue. The ESGM also performs the functions of STF verification and minicell header extraction.

5 Again the EPRM is a dynamic buffer and the allocation/reallocation of slots in this memory is controlled by the egress memory allocation module (EMAM). The dynamic buffer is used to store the received minicells - to absorb jitter, CDV and plesiochronous behaviour an elastic buffering function is performed per ICID under control of the EPMM.

10 The egress payload manager module (EPMM) controls the disassembly of the minicell SDUs to the synchronous timeslots. A connection map (ECMM) identifies the minicell to timeslot associations. The ECMM also performs ancillary functions such as SAD detection. If no minicells are available, or UUI bits indicate a silence period, then the channel activity signal is not asserted. ANP messages may readily use this channel activity to interface to
15 a microprocessor such that available data may be read/written to a SDU and scheduled for despatch or consumed by the microprocessor.

Figure 17 shows a common integrated CPS. Input to the CPS comprises minicells from either ATM or SSCS layers. The output also comprises minicells which are routed to the SSCS or ATM layers accordingly.
20 Incoming minicells are written to the tail of the queue and outgoing minicells are read from the head of the queue. The scheduler controls these processes.

The functional partitioning described above achieves the separation of the functions of CPS packet assembly/switching and the convergence of the
25 minicells stream onto the underlying transport structure. Thus those skilled in the art will recognise that the ATM layer can be replaced by any other regular transport layer (for example MPEG-TS frames). Thus using identical CPS assembly/switching functions one can adapt the invention to operate over any regular transport structure - the use of minicells is therefore not
30 restricted to ATM.

CLAIMS:

1. An adaptation layer switching network in which functional partitioning provides a separation between service specific sublayers (SSCS), common part sublayers (CPS) and transport convergence
5 whereby to support a range of SSCS functions via a common set CPS blocks.
2. An adaptation layer switching network as claimed in claim 1, wherein the network comprises edge device nodes and adaptation layer switching nodes, that the edge nodes terminate the adaptation layer
10 switching nodes to service access points, and wherein the adaptation layer switching nodes provide minicell switching points within the network.
3. An adaptation layer switching network as claimed in claim 2, wherein each said edge device node comprises service modules (SM),
15 adaptation layer switching (ALS) core modules, voice processing modules and physical medium dependent sublayer (PHY) modules, said modules being coupled via an ATM virtual connectivity back plane.
4. An adaptation layer switching network as claimed in claim 3, wherein each said service module is adapted to provide a service
20 specific co-ordination function (SSCF) of adaptation of service information.
5. An adaptation layer switching network as claimed in claim 3 or 4, wherein said physical medium dependent sublayer (PHY) modules are adapted to interface the edge device node to a synchronous or
25 plesiochronous network transport medium.
6. An adaptation layer switching network as claimed in claim 3, wherein each said adaptation layer switching node comprises adaptation layer switching (ALS) core modules and physical medium dependent sublayer (PHY) modules, said modules being coupled via an
30 ATM virtual connectivity back plane.

7. An adaptation layer switching network substantially as described herein with reference to and as shown in the accompanying drawings.
8. A method of functional partitioning of an adaptation layer switching network, the method comprising providing a separation
5 between service specific sublayers (SSCS), common part sublayers (CPS) and transport convergence whereby to support a range of SSCS functions via a common set of CPS blocks.
9. A method of functional partitioning of an adaptation layer switching network substantially as described herein with reference to
10 and as shown in the accompanying drawings.



Application No: GB 9703674.3
Claims searched: 1 to 9

Examiner: Ken Long
Date of search: 23 March 1998

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK CI (Ed.P): H4K (KTK)
H4P (PPS)

Int CI (Ed.6): H04Q (11/04)

Other: ONLINE : WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
X E	EP0786919 A1 IBM (column 6 lines 11-29, column 7 lines 5-14 and column 11 lines 29-40)	1 and 8
X	EP0721267 A2 TOSHIBA (page 8 lines 27-40)	1 and 8
X	EP0708574 A2 ITALTEL (column 1 line 38 to column 2 line 21)	1 and 8
X	Marks D.R.: ATM From A to Z: A Definitive Glossary for Enterprise Network Managers. DATA COMMUNICATIONS, December 1994, pp 113, 114, 116, 118, 120 & 122. (See Figure 1 and the definitions of the terms "Common part convergence sublayer", "Convergence sublayer" and "Service-specific convergence sublayer")	1 and 8

X Document indicating lack of novelty or inventive step
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